Station Groups for Execution Resource Sharing

8 ML Active Stations
8 DEE Active Stations
2 ML columns
2 DEE columns
4 sharing groups

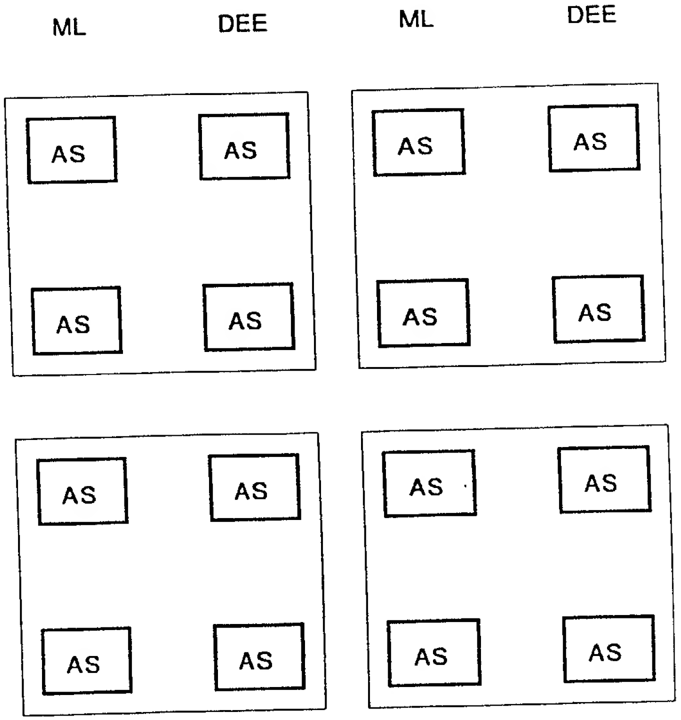


Fig. 1

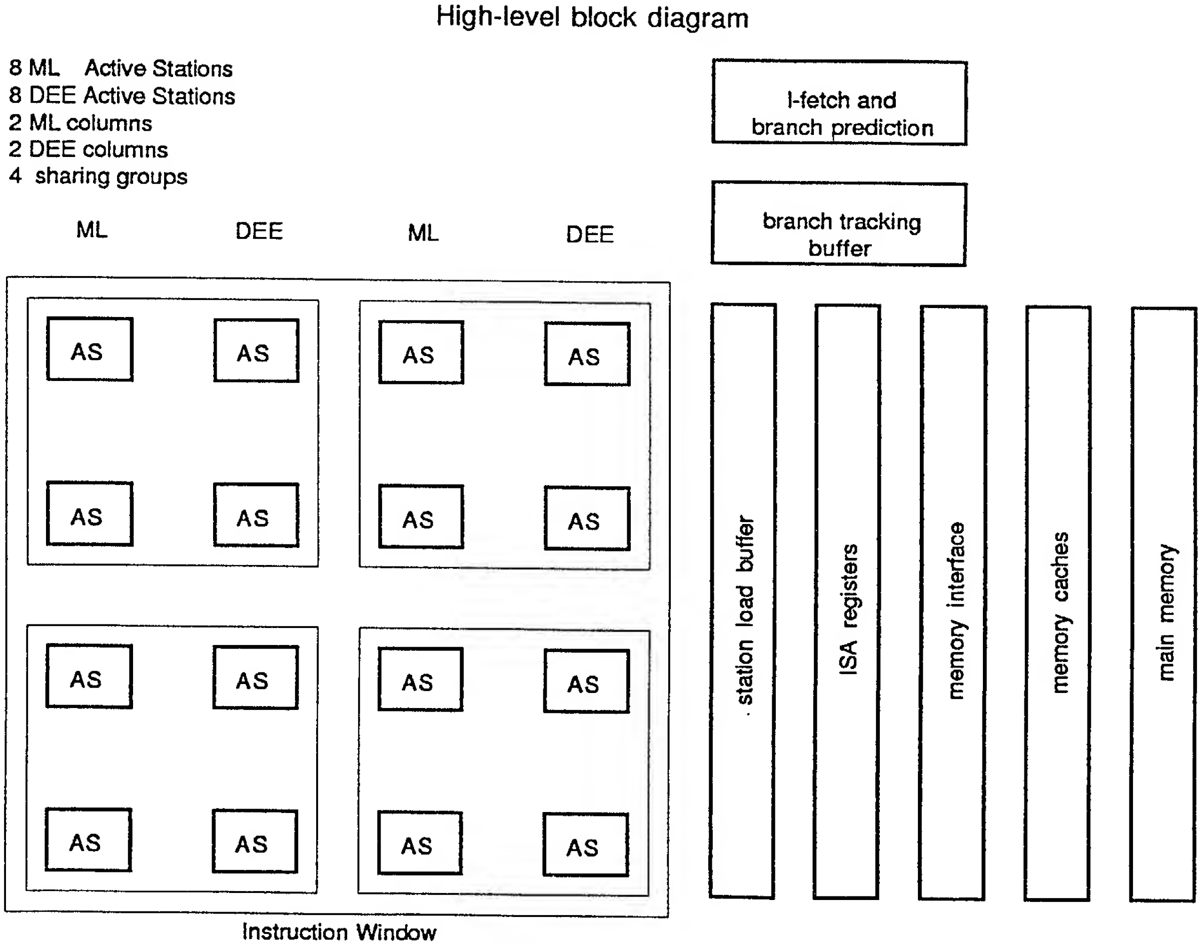

High-level block diagram
8 ML Active Stations
8 DEE Active Stations
2 ML columns
2 DEE columns
4 sharing groups
ML
DEE
ML
DEE
AS
Instruction Window
I-fetch and branch prediction
branch tracking buffer
station load buffer
ISA registers
memory interface
memory caches
main memory

FIG. 2

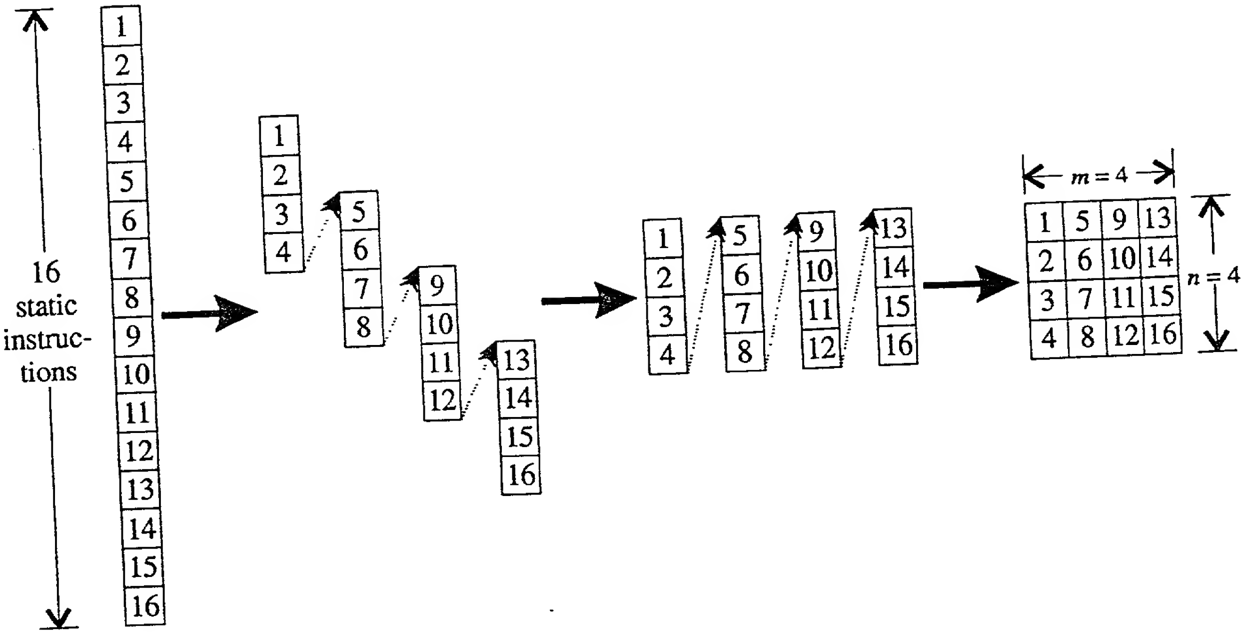
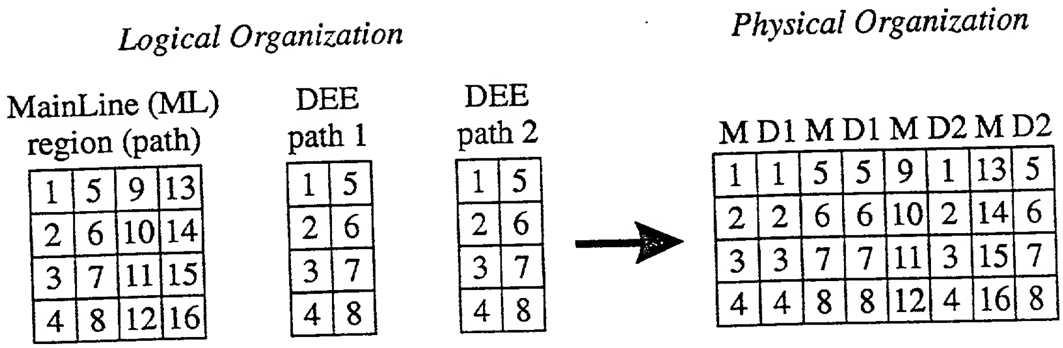


FIG. 3



MainLine (ML) region (path)

1	5	9	13
2	6	10	14
3	7	11	15
4	8	12	16

DEE path 1

1	5
2	6
3	7
4	8

DEE path 2

1	5
2	6
3	7
4	8

Physical Organization

M	D1	M	D1	M	D2	M	D2
1	1	5	5	9	1	13	5
2	2	6	6	10	2	14	6
3	3	7	7	11	3	15	7
4	4	8	8	12	4	16	8

Instruction Window (IW), with Disjoint Eager Execution (DEE)
- each square is an active station -

FIG. 4

ISA Architected Register Files

8 ML Active Stations
8 DEE Active Stations
2 ML columns
2 DEE columns
4 sharing groups

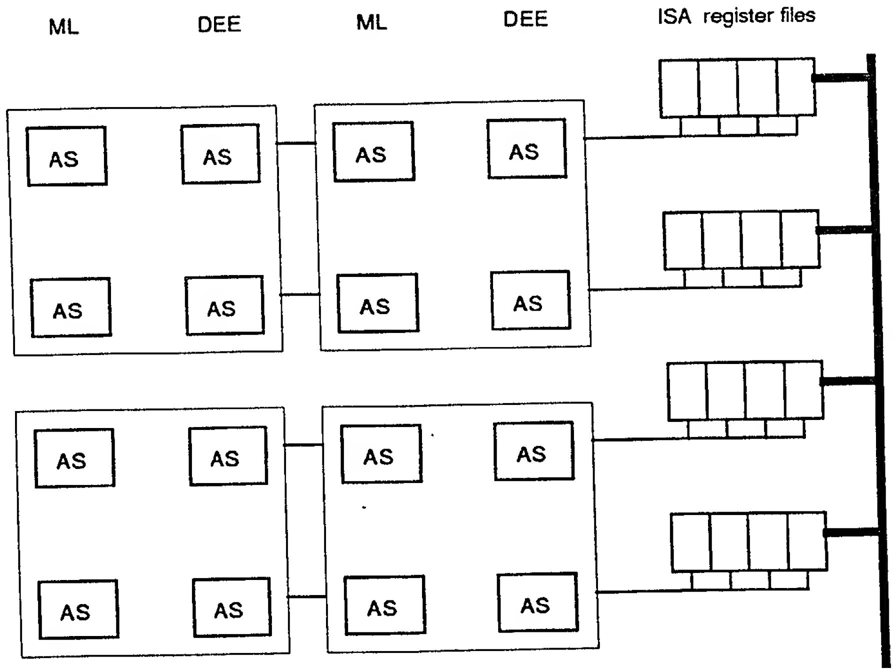


FIG. 5

Memory Interface and Buffers

8 ML Active Stations
8 DEE Active Stations
2 ML columns
2 DEE columns
4 sharing groups

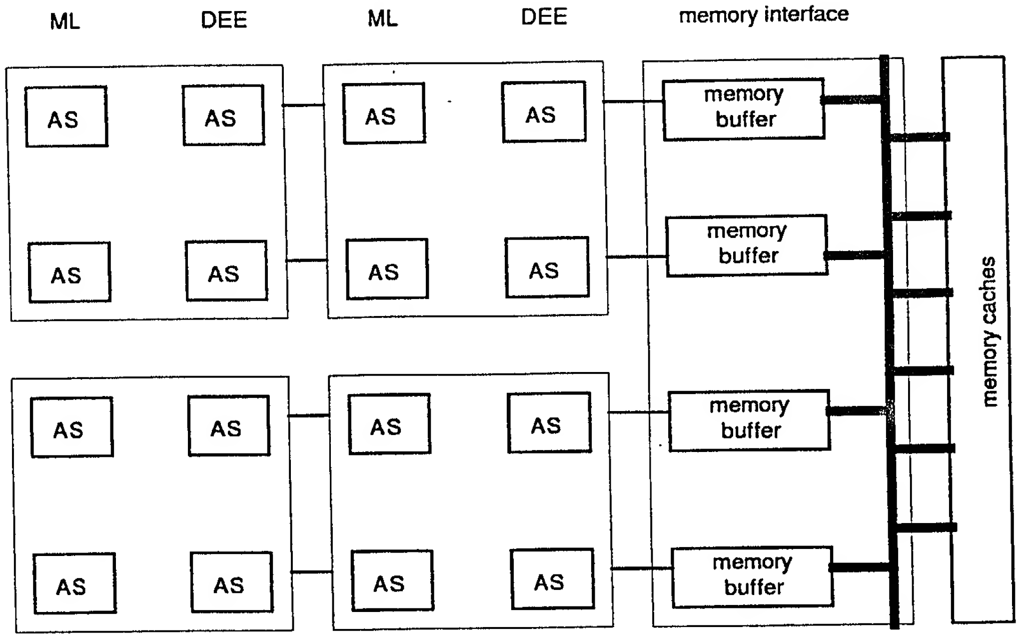


FIG. 6

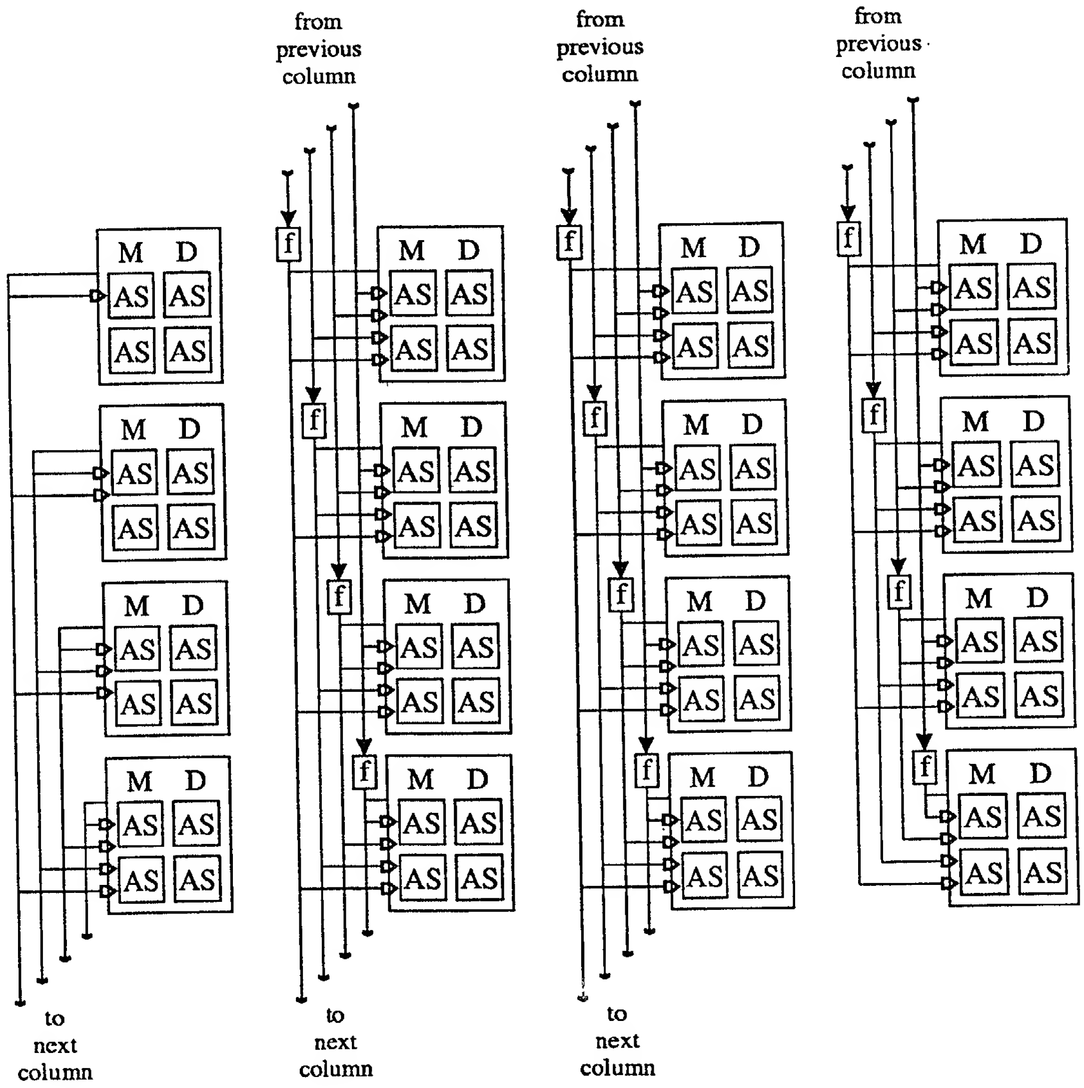

from previous column
from previous column
from previous column
M
D
AS
f
to next column
to next column
to next column

FIG. 7

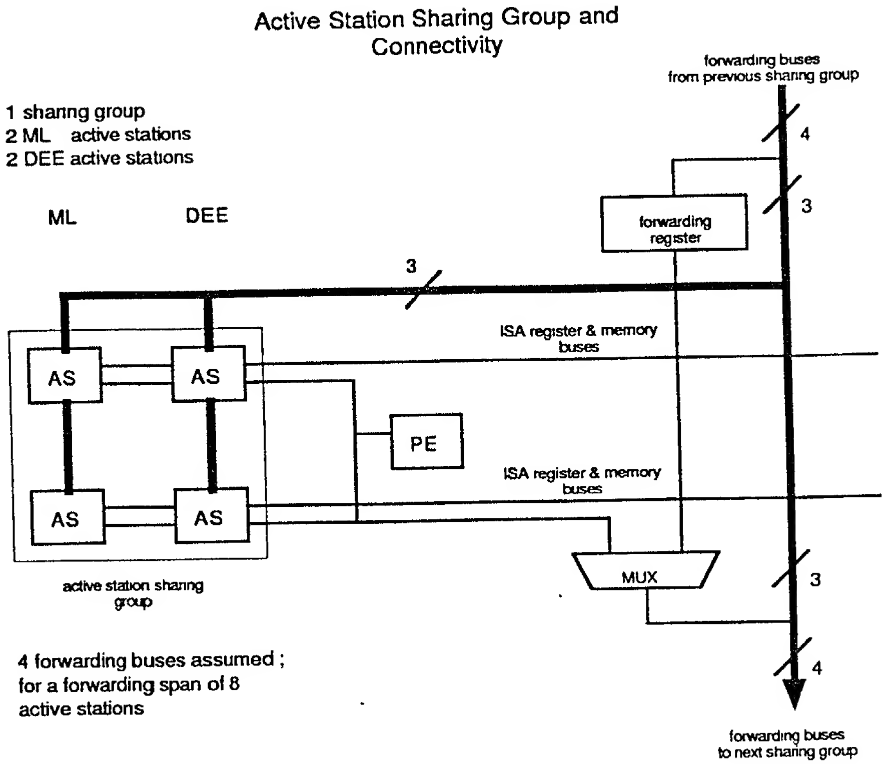

Active Station Sharing Group and Connectivity
1 sharing group
2 ML active stations
2 DEE active stations
ML
DEE
forwarding buses from previous sharing group
4
3
forwarding register
3
AS
AS
AS
AS
PE
ISA register & memory buses
ISA register & memory buses
MUX
3
4
active station sharing group
4 forwarding buses assumed ; for a forwarding span of 8 active stations
forwarding buses to next sharing group

FIG. 8

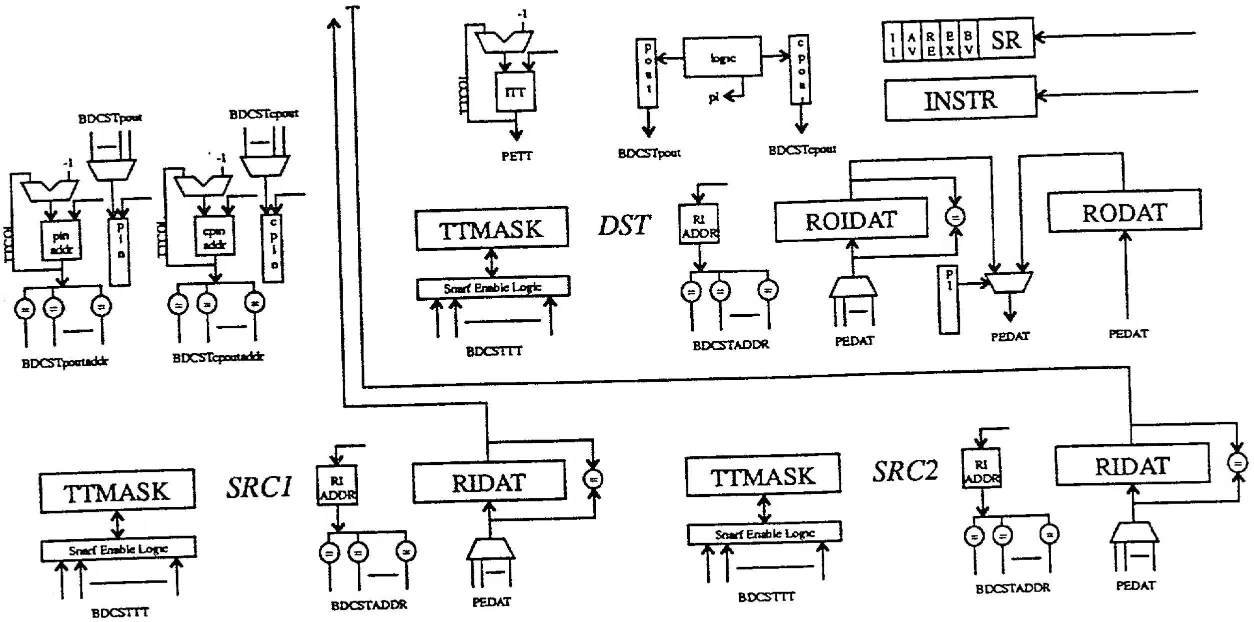

BDCSTpout
BDCSTcpout
-1
TTCOL
pin addr
P i n
cpin addr
c P i n
BDCSTpoutaddr
BDCSTcpoutaddr
-1
TTCOL
ITT
PETT
P o u t
logic
pi
c p o u t
BDCSTpout
BDCSTcpout
I I
A V
R E
E X
B V
SR
INSTR
TTMASK
Snarf Enable Logic
BDCSTTT
DST
RI ADDR
BDCSTADDR
ROIDAT
PEDAT
P I
PEDAT
RODAT
PEDAT
TTMASK
Snarf Enable Logic
BDCSTTT
SRC1
RI ADDR
BDCSTADDR
RIDAT
PEDAT
TTMASK
Snarf Enable Logic
BDCSTTT
SRC2
RI ADDR
BDCSTADDR
RIDAT
PEDAT

FIG. 9

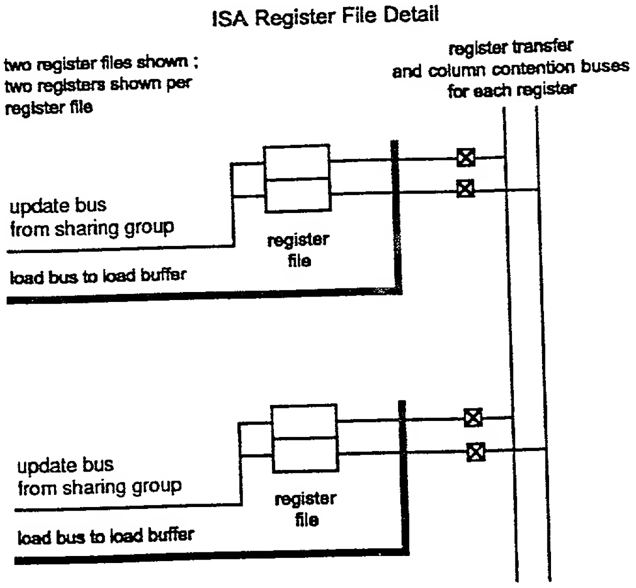

ISA Register File Detail
two register files shown ; two registers shown per register file
register transfer and column contention buses for each register
update bus from sharing group
register file
load bus to load buffer
update bus from sharing group
register file
load bus to load buffer

FIG. 10

time

instruction						
00	X					
10	X					
20	X					
30	X	X				

an 'X' marks an execution

FIG. 11

time

instruction						
00	X					
10	X					
20			X			
30		X		X		

an 'X' marks an execution

FIG. 12

time

instruction						
00		X				
10	X		X			
20	X					
30						

an 'X' marks an execution

FIG. 13

time

instruction	0	1	2	3	4	5	6
00		X				X	
10	X		X				X
20				X			
30		X	X		X		

an 'X' marks an execution

FIG. 14

time

instruction	0	1	2	3	4	5	6
000	X						
010	X		X				
020	X			X			
030	X				X		

an 'X' marks an execution

FIG. 15

time

instruction	0	1	2	3	4	5	6
00	X						
10	X	X					
20	X		R				
30	X						

an 'X' marks an execution, an 'R' marks a relay operation

FIG. 16

time

instruction	0	1	2	3	4	5	6
00			X				
10				X			
20	X				R		
30		X				X	

an 'X' marks an execution, an 'R' marks a relay operation

FIG. 17

time

instruction	0	1	2	3	4	5	6
00	X				X		
10	X	X				X	
20	R		D				B
30	X						

an 'X' marks an execution, an 'R' marks a relay operation, an 'B' marks a broadcast-only operation, a 'D' marks an execution in a DEE path

FIG. 18